REMARKS

Entry of this Amendment is proper because it narrows the issues on appeal and does not require further search by the Examiner.

Claims 11-18 and 26-35 are all the claims presently pending in the application. Claims 11, 15-16, 26 and 32 have been amended to more particularly define the invention. Attached hereto is a marked-up version of the changes made to the claims by the current Amendment.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 15-16 and 32 stand rejected under 35 U.S.C. § 112, first paragraph. Claims 11-12, 18, 26, 28-29 and 33 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Durlam, et al. (U.S. Patent No. 5,940,319). Claims 26, 28 and 33 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Gonzalez, et al. (U.S. Patent No. 6,194,746). Claims 26, 28 and 33 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Aozasa, et al. (U.S. Patent No. 6,065,734). Claims 13-14, 17, 27 and 30-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Durlam, et al., in view of Bronner, et al. (U.S. Patent No. 6,242,770). Claims 34-35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Durlam, et al., in view of Oda (U.S. Patent No. 5,994,749).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (as recited in claim 11) is directed to an array of microelectronic elements which includes a substrate of semiconductor material, a lower layer of dielectric material disposed with a lower surface in contact with the substrate and an upper surface in spaced adjacency thereto, a pattern of mutually electrically isolated conductive regions disposed within the lower layer of dielectric material, the conducting regions extending to the upper surface of the lower layer, an upper layer of dielectric material

disposed with a lower surface thereof in contact with and bonded to the upper surface of the lower layer, and a plurality of nodes of semiconductor material disposed within the upper layer of dielectric material, each of the nodes being in electrical contact with only one of the conducting regions at the upper surface of the lower layer. Importantly, each conducting region includes a metal conductor, and a via formed on the metal conductor and including a diffusion barrier material which contacts a node in the plurality of nodes and electrically connects the metal conductor with the node.

Conventional devices do not include a diffusion barrier between a metal conductor (e.g., a word line) and a semiconductor node (e.g., a silicon diode). Thus, the metal conductor reacts with the semiconductor node, thereby making the devices unreliable. As a result, the metal conductor is commonly made from a refractory metal which has a high resistance.

The claimed invention, on the other hand, includes a via formed on the metal conductor and including a diffusion barrier material which contacts a node in the plurality of nodes and electrically connects the metal conductor with the node. This via may be formed, for example, of refractory metal. The via may act as a diffusion barrier which keeps the conductive region from reacting with the semiconductor material. Therefore, the word lines can be formed of a low resistance metal such as copper and aluminum.

II. THE 35 USC §112, FIRST PARAGRAPH REJECTION

Claims 15-16 and 32 stand rejected under 35 U.S.C. §112, first paragraph as indefinite. Applicant notes, however, that these claims have been amended to address the concerns of the Examiner.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. THE PRIOR ART REFERENCES

A. The Durlam Reference

The Examiner alleges that Durlam teaches the claimed invention as recited in claims 11-12, 18, 26, 28-29 and 33. Applicant submits, however, that there are elements of the

claimed invention which are neither taught nor suggested by Durlam.

Durlam discloses a magnetic random access memory (MRAM) which includes magnetic memory elements. A digit line and bit line are placed under and on top of the memory element. The lines are enclosed by a high permeability layer excluding a surface facing the memory element, which shields and focuses a magnetic field toward the memory element (Durlam at Abstract).

However, contrary to the Examiner's allegations, Durlam does not teach or suggest *"a via formed on said metal conductor and comprising a diffusion barrier material which contacts a node in said plurality of nodes and electrically connects said metal conductor with said node"* as recited, for example, in claim 11 and similarly recited in claim 26. As noted above, conventional devices do not include a diffusion barrier between a metal conductor (e.g., a word line) and a semiconductor node (e.g., a silicon diode). Thus, the metal conductor reacts with the semiconductor node making the devices unreliable. As a result, the metal conductor is commonly made from a refractory metal which has a high resistance. (Application at page 3, lines 3-9; page 8, lines 7-8).

The claimed invention, on the other hand, includes a via formed on the metal conductor and including a diffusion barrier material which contacts a node in the plurality of nodes and electrically connects the metal conductor with the node (Application at page 8, lines 3-16; Figure 5B). This via may be formed, for example, of refractory metal. The via may act as a diffusion barrier which keeps a metal conductor (e.g., word line) from reacting with the semiconductor material (e.g., silicon diode). Therefore, the word lines can be formed of a low resistance metal such as copper and aluminum for improved performance (Application at page 8, lines 3-16).

Clearly, Durlam does not teach or suggest these novel features. Indeed, Durlam does not even discuss at least one of the problems (e.g., reaction between a semiconductor node and a metal conductor (e.g., a word line)) which the claimed invention was intended to address.

The Examiner alleges that the claimed invention is disclosed in Figures 5-8 and 17 of Durlam. However, this is clearly incorrect.

Specifically, the Examiner attempts to equate the metal conductor 37 (Figure 5) and

digit line 82 (Figure 17) with the conductive via of the claimed invention. However, neither of these items in Durlam include a diffusion barrier material which contacts a semiconductor node and electrically connects the metal conductor with the node, as in the claimed invention.

For example, as shown in Figure 5, the metal conductor 37 is connected to the conductor layer 34. In fact, Durlam states that "metal conductors 37 and 38 which are employed to electrically connect plug conductors 19a and 19b to conductor layer 34" (Durlam at col. 3, line 65-col. 4, line 1). Certainly, the "conductor" layer 34 cannot be mistaken for a "semiconductor". Thus, it is clear that the metal 37 in Durlam does not connect a metal conductor to a semiconductor.

Further, the Examiner must understand that one important purpose of the via is to prevent the underlying metal conductor from reacting with a semiconductor node, such as a silicon diode. In Durlam, there is no semiconductor which would be contacting the plug conductor 19a, only conductor layer 34. Thus, there would be no problem with a reaction between conductor layer 34 and plug conductor 19a. Therefore, there would be no reason to insert a conductive via including diffusion barrier material therebetween.

It is equally unreasonable to equate the digit lines 82 shown in Figure 17 in Durlam, with the conductive via of the claimed invention. For example, the metal conductor 82 in the Durlam device is formed of Al or Cu or their alloys (Durlam at col. 6, lines 36-38; col. 3, lines 35-38; Figures 3, 4 and 17). Thus, as shown in Figure 17, Durlam teaches forming the diodes 93 and 95 directly on the Al and Cu. As explained in the Application, Al and Cu is reactive with the semiconductor and therefore, the Durlam structure would result in an unreliable device. Indeed, one advantage provided by the conductive via in the claimed invention is that the via may act as a diffusion barrier to prevent a conductor such as Cu or Al from reacting with a semiconductor diode formed thereon.

Moreover, the digit line 82 can not reasonably be considered a "via". Indeed, it is formed on a substrate 81 and does not connect two conductive elements. Thus, it is clearly unrelated to the conductive via in the claimed invention which includes a diffusion barrier material which contacts a semiconductor node and electrically connects the metal conductor with the node. Therefore, contrary to the Examiner's allegations, Durlam is clearly unrelated to the claimed invention.

not taught or suggest by Durlam. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Gonzalez Reference

The Examiner alleges that Gonzalez teaches the claimed invention as recited in claims 26, 28 and 33. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Gonzalez.

Gonzalez discloses a vertical diode having a diode opening extending through an insulation layer and contacting an active region on a silicon wafer. The diode opening is initially filled with an amorphous silicon plug that is doped during deposition and subsequently recrystallized to form large grain polysilicon. A programmable resistor contacts the top portion of the silicon plug and a metal line contacts the programmable resistor (Gonzalez at Abstract).

However, contrary to the Examiner's allegations, Durlam does not teach or suggest "*a via formed on said metal conductor and comprising a diffusion barrier material which contacts a node in said plurality of nodes and electrically connects said metal conductor with said node*" as similarly recited in claim 26. As noted above, unlike conventional devices which do not include a diffusion barrier between a metal conductor (e.g., a word line) and a semiconductor node (e.g., a silicon diode), the claimed invention includes a via formed on the metal conductor and including a diffusion barrier material which contacts a node in the plurality of nodes and electrically connects the metal conductor with the node (Application at page 8, lines 3-16; Figure 5B).

The conductive via may be formed, for example, of refractory metal. The via may act as a diffusion barrier which keeps a metal conductor (e.g., word line) from reacting with the semiconductor material (e.g., silicon diode). Therefore, the word lines can be formed of a low resistance metal such as copper and aluminum (Application at page 8, lines 3-16) for improved performance.

Clearly, Gonzalez does not teach or suggest these novel features. Indeed, Gonzalez does not even discuss at least one of the problems (e.g., reaction between a semiconductor node and a metal conductor (e.g., a word line)) which the claimed invention was intended to

address.

The Examiner alleges that the claimed invention is disclosed in Figure 30 of Gonzalez. However, this is clearly incorrect.

Specifically, the Examiner attempts to equate the tungsten plug 162 in Gonzalez with the conductive via of the claimed invention. However, clearly the tungsten plug 162 is not formed on a metal conductor and does not contact a semiconductor node and electrically connect the metal conductor with the node, as in the claimed invention.

Indeed, as clearly shown in Figure 30, the tungsten plug 162 contacts programmable resistor 164 (or another tungsten plug 176) with p-doped silicon 152 (Gonzalez at Figure 30; col. 14, lines 60-64). The programmable resistor is formed of memory material such as chalcogenide (which may or may not include a metal) (Gonzalez at col. 8, lines 35-40).

However, the tungsten plug 162 is formed on the p-doped polysilicon 152 and both surrounded by silicon oxide 156 (Gonzalez at col. 15, lines 4-8). The programmable resistor 164 is then formed on the tungsten plug 162, and another oxide layer 168 is then formed over the programmable resistor 164 (Gonzalez at col. 15, lines 44-55).

Therefore, unlike the claimed invention in which a via is formed on a metal conductor in a lower dielectric, and contacts a semiconductor node in an upper dielectric layer, Gonzalez teaches a tungsten plug 162 formed on p-doped polysilicon 152 together in one oxide layer 156, and contacting the programmable resistor 164 (which may or may not contain metal) which is formed in a separate oxide layer 168 which is deposited on (not bonded to, as alleged by the Examiner) the oxide layer 156. Therefore, the Gonzalez device is clearly unrelated to the claimed invention.

Again, the Examiner must understand that one important purpose of the via is to prevent the underlying metal conductor from reacting with a semiconductor node, such as a silicon diode. In Gonzalez, the tungsten plug clearly does not serve that purpose.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Gonzalez. Therefore, the Examiner is respectfully requested to withdraw this rejection.

C. The Aozasa Reference

The Examiner alleges that Aozasa teaches the claimed invention as recited in claims 26, 28 and 32. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Aozasa.

Aozasa discloses a non-volatile memory device in which the gate electrodes are formed on an upper surface and a lower surface of the channel via insulating layers, respectively, one used as a read electrode and the other used as a write electrode (Aozasa at Abstract).

However, contrary to the Examiner's allegations, Aozasa does not teach or suggest "*a via formed on said metal conductor and comprising a diffusion barrier material which contacts a node in said plurality of nodes and electrically connects said metal conductor with said node*" as similarly recited in claim 26. As noted above, the conductive via may be formed, for example, of refractory metal. The via may act as a diffusion barrier which keeps a metal conductor (e.g., word line) from reacting with the semiconductor material (e.g., silicon diode). Therefore, the word lines can be formed of a low resistance metal such as copper and aluminum (Application at page 8, lines 3-16) for improved performance.

Clearly, Aozasa not teach or suggest these novel features. Indeed, Aozasa does not even discuss at least one of the problems (e.g., reaction between a semiconductor node and a metal conductor (e.g., a word line)) which the claimed invention was intended to address.

The Examiner alleges that the claimed invention is disclosed in Figure 23 of Aozasa. However, this is clearly incorrect.

Specifically, Aozasa discloses an insulating layer 206 and interlayer insulation 244 (Aozasa at Figure 23). In the insulating layer 206 is formed a semiconductor layer which includes a source region 220 and drain region 222 of a memory cell (Aozasa at col. 12, lines 22-29).

The Examiner seems to equate the gate electrode 216 in the Aozasa device with the conductive via of the claimed invention. However, the gate electrode 216 in Aozasa clearly does not include a conductive via. Further, in the claimed invention, the via may be in electrical contact with a semiconductor node (Application at Figure 5B). However, in Aozasa, the gate electrode 216 is merely in contact with the insulation 206 and the gate

insulation 283d (Aozasa at Figure 23).

In addition, in the claimed invention, the semiconductor nodes may be formed in a second dielectric layer which may be bonded to first dielectric layer having the conductive regions. However, in Aozasa, the semiconductor layer (e.g., source and drain regions 220, 222) above the gate insulation 283 is formed in the same insulation 206 as the gate electrode 216 which the Examiner equates with the conductive via of the claimed invention. Clearly, these devices are completely unrelated.

Again, the Examiner must understand that one important purpose of the via is to prevent the underlying metal conductor from reacting with a semiconductor node, such as a silicon diode. In Aozasa, the gate electrode 216 clearly does not serve that purpose.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Aozasa. Therefore, the Examiner is respectfully requested to withdraw this rejection.

D. The Bronner Reference

The Examiner alleges that Durlam would have been combined with Bronner to form the claimed invention as recited in claims 13-14, 17, 27 and 30-31. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Bronner discloses a magneto-resistive memory cell which includes a substrate, monocrystalline diode formed in the substrate, a first conductor in the substrate and a second conductor formed above a magnetic tunnel junction formed on the diode (Bronner at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different matters. Specifically, the Durlam device is merely intended to prevent a magnetic memory element from thermal degradation during fabrication (Durlam at col. 1, lines 61-64), whereas Bronner is intended to minimize the resistance of a diode in a memory cell (Bronner at col. 3, lines 3-4). Clearly, no person of ordinary skill in the art would have considered combining these references.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that "[i]t would have been obvious to form Durlam's diodes as single crystal Si diodes because according to Bronner, such single crystal Si diodes ... would provide high conductivity, high rectification, and low total resistance" which is insufficient to support the combination.

Moreover, Bronner does not teach or suggest "*a via formed on said metal conductor and comprising a diffusion barrier material which contacts a node in said plurality of nodes and electrically connects said metal conductor with said node*" as recited, for example, in claim 11 and similarly recited in claim 26. As noted above, the conductive via may be formed, for example, of refractory metal. The via may act as a diffusion barrier which keeps a metal conductor (e.g., word line) from reacting with the semiconductor material (e.g., silicon diode). Therefore, the word lines can be formed of a low resistance metal such as copper and aluminum (Application at page 8, lines 3-16) for improved performance.

Clearly, Bronner does not teach or suggest the novel features of the claimed invention. Indeed, Bronner does not even discuss at least one of the problems (e.g., reaction between a semiconductor node and a metal conductor (e.g., a word line)) which the claimed invention was intended to address.

Further, Bronner may disclose a single crystal Si diode, but Bronner clearly does not form the diode in electrical contact with a via. Indeed, in Bronner, the diode 514 is in the shaped of a V-groove formed in an insulation layer100. A metal conductor 525 is formed on the diode 514 and an oxide layer 530 is formed on the metal conductor 525 (Bronner at Figure 5B). This is completely unrelated to the claimed invention. Thus, Bronner clearly does not make up for the deficiencies of Durlam.

Again, the Examiner must understand that one important purpose of the via is to prevent the underlying metal conductor from reacting with a semiconductor node, such as a silicon diode. Bronner clearly does not teach or suggest a via that is intended to serve that purpose.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the

claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

E. The Oda Reference

The Examiner alleges that Oda would have been combined with Durlam to form the claimed invention as recited in claims 34-35. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Oda discloses a semiconductor device which includes a semiconductor substrate having an element region and source and drain regions, a gate dielectric film containing nitrogen formed in the element region of said semiconductor substrate, a gate electrode formed on the gate dielectric film a first dielectric film formed adjacent to the gate electrode so as to define a side wall therefor, a second dielectric film formed so as to cover the gate electrode and the first dielectric film, the second dielectric film being doped with nitrogen, and a third dielectric film formed so as to cover the second dielectric film, the third dielectric film being formed of silicon nitride (Oda at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different matters. Specifically, the Durlam device is merely intended to prevent a magnetic memory element from thermal degradation during fabrication (Durlam at col. 1, lines 61-64), whereas Oda is merely intended to prevent nitrogen from diffusing out of a gate oxide and gate electrode (Oda at col. 3, lines 5-23). Clearly, no person of ordinary skill in the art would have considered combining these references.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that "[i]t would have been obvious to form Durlam's diodes as single crystal Si diodes because according to Bronner, such single crystal Si diodes ... would provide high conductivity, high rectification, and low total resistance" which is insufficient to support the combination.

Moreover, like the other references, Oda does not teach or suggest "*a via formed on*

said metal conductor and comprising a diffusion barrier material which contacts a node in said plurality of nodes and electrically connects said metal conductor with said node" as similarly recited in claim 26. As noted above, the conductive via may be formed, for example, of refractory metal. The via may act as a diffusion barrier which keeps a metal conductor (e.g., word line) from reacting with the semiconductor material (e.g., silicon diode). Therefore, the word lines can be formed of a low resistance metal such as copper and aluminum (Application at page 8, lines 3-16) for improved performance.

Clearly, Oda not teach or suggest these novel features. Indeed, Oda does not even discuss at least one of the problems (e.g., reaction between a semiconductor node and a metal conductor (e.g., a word line)) which the claimed invention was intended to address.

Further, the Examiner attempts to equate the tungsten plug 18 in Oda with the conductive via of the claimed invention. However, this is clearly incorrect.

Specifically, in Oda, the tungsten plug 18 connects an aluminum alloy wiring layer 14 to another aluminum alloy wiring layer 19 (Oda at Figure 1; col. 5, lines 15-32). This is clearly contrary to the claimed invention, in which the via may connect a metal conductor with a semiconductor node. Thus, Oda clearly does not make up for the deficiencies of Durlam.

Again, the Examiner must understand that one important purpose of the via is to prevent the underlying metal conductor from reacting with a semiconductor node, such as a silicon diode. Oda clearly does not teach or suggest a via that is intended to serve that purpose.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 11-18 and 26-35, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above

10/080,568
YOR919980324US2

and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 5/27/03

Phillip E. Miller
Registration No. 46,060

FAX RECEIVED
MAY 27 2003
TECHNOLOGY CENTER 2800

McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Amendment was filed by facsimile with the United States Patent and Trademark Office, Examiner Phat X. Cao, Group Art Unit # 2814 at fax number (703)872-9319 this 27th day of May, 2003.

Phillip E. Miller
Registration No. 46,060

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims to read as follows:

11. (Amended) An array of microelectronic elements comprising:

a substrate of semiconductor material; [,]

a lower layer of dielectric material disposed with a lower surface in contact with said substrate and an upper surface in spaced adjacency thereto; [,]

a pattern of mutually electrically isolated conducting regions [metal conductors] disposed within said lower layer of dielectric material, said [metal conductors comprising a plurality of spaced apart] conducting regions extending to said upper surface of said lower layer; [,]

an upper layer of dielectric material disposed with a lower surface thereof in contact with and bonded to said upper surface of said lower layer; [,] and

a plurality of nodes of semiconductor material disposed within said upper layer of dielectric material, each of said nodes being in electrical contact with only one of said conducting regions at said upper surface of said lower layer,

wherein each conducting region comprises:

a metal conductor; and

a via formed on said metal conductor and comprising a diffusion barrier [an electrically conducting] material which contacts a node in said plurality of nodes and electrically connects said metal conductor [, each node being in electrical contact] with said node [via].

15. (Amended) An array as set forth in claim 12, wherein said semiconductor device comprises [is] a field effect transistor [comprising a first gate electrode in contact with one of said conducting regions at said upper surface of said lower layer].

16. (Amended) An array as set forth in claim 15, wherein a first insulating layer is disposed over an upper surface of said upper layer and a second insulating layer is formed over said upper surface of said lower layer [, and wherein a second gate electrode is deposited

upon said first insulating layer above each field effect transistor].

26. (Amended) A microelectronic element array comprising:

a semiconductor substrate;

a first dielectric layer formed on said substrate;

a plurality of electrically isolated conductive regions disposed within said first dielectric layer, each conductive region comprising:

a metal conductor; and

a conductive via comprising a diffusion barrier material formed on said metal conductor;

a second dielectric layer having a lower surface which is bonded to an upper surface of said first dielectric layer; and

a plurality of semiconductor nodes formed in said second dielectric layer, each semiconductor node contacting said conductive via and being electrically connected to said metal conductor by [in electrical contact with] said conductive via.

32. (Amended) The array according to claim 26, further comprising:

a plurality of field effect transistors, each node in said plurality of semiconductor nodes forming a part of each field effect transistor[,

wherein each field effect transistor forms a memory element].